IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:

Krishna Rangasayee et al.

Serial No.:

08/707,694

Title:

INTEGRATED PHASE LOCK LOOP

Filed:

September 4, 1996

Attorney Docket No.:

Butler, D.

0325.00063

Art Unit:

Examiner:

2787

In Response To:

Office Action mailed December 2, 1997

PROGRAMMABLE LOGIC DEVICE HAVING AN

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on March 2, 1998.

<u>AMENDMENT</u>

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

In response to the Office Action mailed December 2, 1997, please amend the above-identified application as follows:

IN THE SPECIFICATION

Page 1, line 7, replace "(PLD's)" with -- (PLDs) --.

Page 1, line 14, replace "on board" with --on-board--.

Page 2, line 9, after "implements", insert --,--.